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1	4271	tlb or (translation adj2 buffer)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/13 15:34
2	759	atb or dlat	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/13 15:34
3	2347	(lookaside or look-aside) adj (table or buffer)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/13 15:36
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6	15	coherency near5 ((lookaside or look-aside) adj (table or buffer))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/13 15:36
7	2	(coherency near5 ((lookaside or look-aside) adj (table or buffer))) not (coherency near5 (tlb or (translation adj2 buffer)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/02/13 15:36
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1 **A 90 MHz CMOS RISC CPU designed for sustained performance**
Tanksalvala, D.; Lamb, J.; Buckley, M.; Long, B.; Chapin, S.; Lotz, J.; Delano, E.; Luebs, R.; Erskine, K.; McMullen, S.; Forsyth, M.; Novak, R.; Gaddis, T.; Quarnstrom, D.; Gleason, C.; Rashid, E.; Halperin, D.; Sigel, L.; Hill, H.; Simpson, C.; Hollenbe
Solid-State Circuits Conference, 1990. Digest of Technical Papers.
37th ISSCC., 1990 IEEE International , 14-16 Feb 1990
Page(s): 52 -53, 264

[Abstract]   [PDF Full-Text (880 KB)] **IEEE CNF**

2 **A 2-ns, 5-mW, synchronous-powered static-circuit fully associative TLB**
Higuchi, H.; Tachibana, S.; Minami, M.; Nagano, T.;
VLSI Circuits, 1995. Digest of Technical Papers., 1995 Symposium on , 8-10 Jun 1995
Page(s): 21 -22

[Abstract]   [PDF Full-Text (240 KB)] **IEEE CNF**

3 **Multi-threading and remote latency in software DSMs**
Thitikamol, K.; Keleher, P.;
Distributed Computing Systems, 1997., Proceedings of the 17th
International Conference on , 27-30 May 1997
Page(s): 296 -304

[Abstract]   [PDF Full-Text (1084 KB)] **IEEE CNF**

4 **Lazy TLB consistency for large-scale multiprocessors**

Moon-Seek Chang; Kern Koh;
Parallel Algorithms/Architecture Synthesis, 1997. Proceedings. Second
Aizu International Symposium , 17-21 Mar 1997
Page(s): 308 -315

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1 **A memory management unit and cache controller for the MARS system**
Feipei Lai; Chyuan-Yow Wu; Tai-Ming Parng;
Microprogramming and Microarchitecture. Micro 23. Proceedings of the 23rd Annual Workshop and Symposium., Workshop on , 27-29 Nov 1990
Page(s): 200 -208

[Abstract]   [PDF Full-Text (772 KB)] **IEEE CNF**

2 **The next-generation SPARC multiprocessing system architecture**
Frailong, J.-M.; Cekleov, M.; Sindhu, P.; Gastinel, J.; Splain, M.; Price, J.; Singhal, A.;
Compcon Spring '93, Digest of Papers. , 22-26 Feb 1993
Page(s): 475 -480

[Abstract]   [PDF Full-Text (496 KB)] **IEEE CNF**

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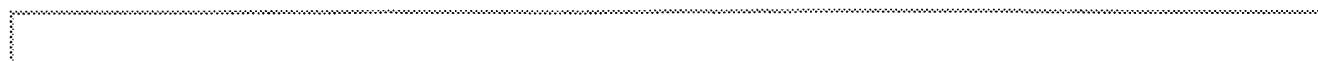
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hierarchy
W. H. Wang , J.-L. Baer , H. M. Levy
ACM SIGARCH Computer Architecture News , Proceedings of the
16th annual international symposium on Computer architecture April
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Donald Yeung , John Kubiatowicz , Anant Agarwal
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Dimitrios S. Nikolopoulos , Theodore S. Papatheodorou , Constantine
D. Polychronopoulos , Jesús Labarta , Eduard Ayguadé
Proceedings of the 14th international conference on Supercomputing
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Mary Hall , Peter Kogge , Jeff Koller , Pedro Diniz , Jacqueline

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Hongzhang Shan , Jaswinder Pal Singh
Proceedings of the 1999 ACM/IEEE conference on Supercomputing (CDROM) January 1999

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Dileep Bhandarkar , Richard Brunner
ACM SIGARCH Computer Architecture News , Proceedings of the 17th annual international symposium on Computer Architecture May 1990
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Kazuaki Murakami , Shin-ichiro Mori , Akira Fukuda , Toshinori Sueyoshi , Shinji Tomita
Proceedings of the 3rd international conference on Supercomputing June 1986

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Christoph Kern , Mark R. Greenstreet
ACM Transactions on Design Automation of Electronic Systems (TODAES) April 1999
Volume 4 Issue 2

9 Comparing the memory system performance of the HP V-class   100%
and SGI Origin 2000 multiprocessors using microbenchmarks
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Ravi Iyer , Nancy M. Amato , Lawrence Rauchwerger , Laxmi Bhuyan
Proceedings of the 13th international conference on Supercomputing May 1999

10 Options for dynamic address translation in COMAs   100%
Xiaogang Qiu , Michel Dubois
ACM SIGARCH Computer Architecture News , Proceedings of the 25th annual international symposium on Computer architecture April 1998
Volume 26 Issue 3

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Feipei Lai , Chyuan-Yow Wu , Tai-Ming Parng
Proceedings of the 23rd annual workshop and symposium on
Microprogramming and microarchitecture November 1990

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Babak Falsafi , David A. Wood
ACM Transactions on Modeling and Computer Simulation (TOMACS)
January 1997
Volume 7 Issue 1

13 SoftFLASH: analyzing the performance of clustered distributed   100%
virtual shared memory
Andrew Erlichson , Neal Nuckolls , Greg Chesson , John Hennessy
Proceedings of the seventh international conference on Architectural
support for programming languages and operating systems
September 1996

14 High-bandwidth address translation for multiple-issue   100%
processors
Todd M. Austin , Gurindar S. Sohi
ACM SIGARCH Computer Architecture News , Proceedings of the
23rd annual international symposium on Computer architecture May
1996
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15 MGS: a multigrain shared memory system   100%
Donald Yeung , John Kubiatowicz , Anant Agarwal
ACM SIGARCH Computer Architecture News , Proceedings of the
23rd annual international symposium on Computer architecture May
1996
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architecture-dependent micro optimization
Jochen Liedtke , Kevin Elphinstone
ACM SIGOPS Operating Systems Review January 1996
Volume 30 Issue 1

17 Software versus hardware shared-memory implementation: a   100%
case study

A. L. Cox , S. Dwarkadas , P. Keleher , H. Lu , R. Rajamony , W. Zwaenepoel
ACM SIGARCH Computer Architecture News , Proceedings of the 21ST annual international symposium on Computer architecture
April 1994
Volume 22 Issue 2

18 An in-cache address translation mechanism   100%
D. A. Wood , S. J. Eggers , G. Gibson , M. D. Hill , J. M. Pendleton
ACM SIGARCH Computer Architecture News , Proceedings of the 13th annual international symposium on Computer architecture June 1986
Volume 14 Issue 2

19 Limits to low-latency communication on high-speed networks   100%
Chandramohan A. Thekkath , Henry M. Levy
ACM Transactions on Computer Systems (TOCS) May 1993
Volume 11 Issue 2

20 Executing compressed programs on an embedded RISC   100%
architecture
Andrew Wolfe , Alex Chanin
ACM SIGMICRO Newsletter , Proceedings of the 25th annual international symposium on Microarchitecture December 1992
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1 **TLB consistency on highly-parallel shared-memory multiprocessors**
Teller, P.J.; Kenner, R.; Snir, M.;
System Sciences, 1988. Vol.I. Architecture Track, Proceedings of the Twenty-First Annual Hawaii International Conference on , 5-8 Jan 1988
Page(s): 184 -193

[Abstract]   [PDF Full-Text (888 KB)] **IEEE CNF**

2 **A simple, extendible ATM switch with load-balanced rounding copy network**
Taeck-Geun Kwon; Choong-Kyo Jeong;
Communications, 1995. ICC 95 Seattle, Gateway to Globalization, 1995 IEEE International Conference on , Volume: 2 , 18-22 Jun 1995
Page(s): 1122 -1126 vol.2

[Abstract]   [PDF Full-Text (400 KB)] **IEEE CNF**

3 **Lazy TLB consistency for large-scale multiprocessors**
Moon-Seek Chang; Kern Koh;
Parallel Algorithms/Architecture Synthesis, 1997. Proceedings. Second Aizu International Symposium , 17-21 Mar 1997
Page(s): 308 -315

[Abstract]   [PDF Full-Text (724 KB)] **IEEE CNF**

4 **Group contexts: an architectural approach to virtual sharing**

Mohamed, A.; Sagahyroon, A.;
Communications, Computers and Signal Processing, 1997. '10 Years
PACRIM 1987-1997 - Networking the Pacific Rim'. 1997 IEEE Pacific
Rim Conference on , Volume: 1 , 20-22 Aug 1997
Page(s): 289 -293 vol.1

[Abstract]   [PDF Full-Text (552 KB)] **IEEE CNF**

5 Options for dynamic address translation in COMAs
Xiaogang Qiu; Dubois, M.;
Computer Architecture, 1998. Proceedings. The 25th Annual
International Symposium on , 27 Jun-1 Jul 1998
Page(s): 214 -225

[Abstract]   [PDF Full-Text (76 KB)] **IEEE CNF**

6 The role of breast compression in scintimammography
*Pani, R.; Pellegrini, R.; Solouri, A.; Weinberg, I.N.; De Vincentis, G.;
Scafe, R.; Cinti, M.N.; Betti, M.; Inches, R.; Scopinaro, F.; Garibuldi,
F.; Cusanno, F.; Del Guerra, A.; Khalkhali, I.;*
Nuclear Science Symposium Conference Record, 2000 IEEE , Volume:
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Page(s): 21/98 -21100 vol.3

[Abstract]   [PDF Full-Text (216 KB)] **IEEE CNF**

7 A VLSI chip set for a multiprocessor workstation. II. A memory management unit and cache controller
*Jeong, D.-K.; Wood, D.A.; Gibson, G.A.; Eggers, S.J.; Hodges, D.A.;
Katz, R.H.; Patterson, D.A.;*
Solid-State Circuits, IEEE Journal of , Volume: 24 Issue: 6 , Dec 1989
Page(s): 1699 -1707

[Abstract]   [PDF Full-Text (916 KB)] **IEEE JNL**

8 Translation-lookaside buffer consistency
Teller, P.J.;
Computer , Volume: 23 Issue: 6 , Jun 1990
Page(s): 26 -36

[Abstract]   [PDF Full-Text (1028 KB)] **IEEE JNL**

9 On achieving complete fault coverage for sequential machines
Pomeranz, I.; Reddy, S.M.;

Computer-Aided Design of Integrated Circuits and Systems, IEEE
Transactions on , Volume: 13 Issue: 3 , Mar 1994
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